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Passivation and Gating of GaAs and Si Surfaces Using Pseudomorphic Structures

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This program explores MISFET structures in material systems with no suitable native oxide. This has included GaAs, and in this latest period Ge. A novel structure has been developed utilizing a thin (<15 Å) epitaxial layer of Si to control the chemical interface formed by deposition of SiO_2. Detailed characterization of the interfacial chemistry is presented along with p-channel MISFET results. A room temperature, p-channel transconductance of 52 mS/mm was measured at a gate length of 2 μm; along with a peak effective hole mobility of 430 $cm^2V^{-1}sec^{-1}$.

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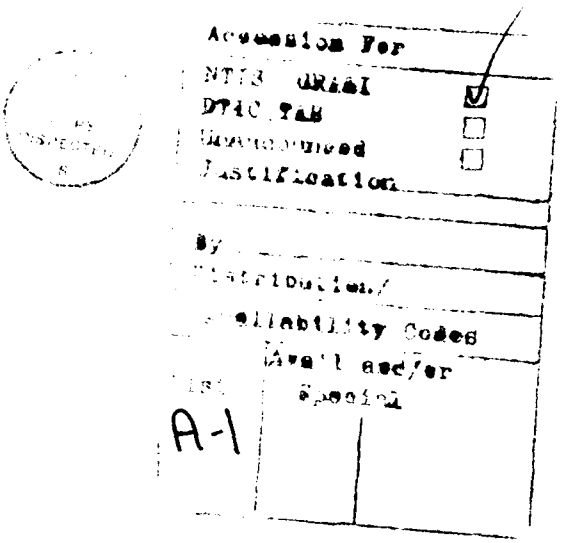

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SUMMARY

Recent studies [Hattangady *et al*, Appl. Phys. Lett. **57**(6), 581 (1990)] have shown greatly reduced interface state densities (5×10^{10} cm^{-2} eV^{-1}) in Ge-based, metal-insulator-semiconductor structures with the use of an ultrathin, pseudomorphic Si interlayer between the gate dielectric, SiO_2, and the Ge semiconductor substrate. The Si and the SiO_2 layers are deposited *in situ* and sequentially at low temperature (300°C) in a remote plasma-enhanced chemical vapor deposition system. This report presents an analysis of the Si-Ge heterostructure before and after the SiO_2 deposition. Low energy He ion scattering spectroscopy shows that the silicon layer (28 Å) provides complete coverage of the Ge surface prior to the deposition of the SiO_2 film. The existence of the silicon interlayer *after* the remote-plasma enhanced deposition of 150 Å of the SiO_2 film is established by x-ray photoelectron spectroscopy (XPS). Throughout a cumulative series of thin (~10 Å) oxide depositions, XPS showed no evidence of Ge oxidation states other than Ge^{0+} (elemental Ge) at the interface. Quantitative XPS has been used to evaluate the extent of *subcutaneous oxidation* which could determine the amount of Si remaining at the interface and thereby influence the electrical properties of the semiconductor-oxide interface. For the conditions studied, it is observed that oxidation consumes only 4 Å of the initial 28 Å of silicon. Furthermore, this is apparently due to the plasma oxidation of the silicon at the *initiation* of the remote oxygen plasma discharge. Subcutaneous oxidation is limited thereafter by the oxide film that forms a barrier to oxygen diffusion. In addition, the XPS analysis reveals several important characteristics of SiO_2-Si interface formation with these plasma-deposited SiO_2 dielectric films. Inversion mode, *p*-channel Ge field-effect-transistors fabricated with this

composite SiO_2-Si gate dielectric structure show a maximum room temperature transconductance of 52 mS mm^{-1} at a gate length of 2 μm and a peak effective channel hole mobility of 430 cm^2 V^{-1} s^{-1}. These devices exhibit negligible charge-induced threshold shifts.

I. INTRODUCTION

A novel insulator structure involving the use of an ultrathin, pseudomorphic Si interlayer between the semiconductor and the gate dielectric, SiO_2, was proposed recently for Ge metal-insulator-semiconductor (MIS) structures[1-4]. The primary motivation to explore the utility of such a structure was derived simply from (a) the observation that Si forms an excellent electrical interface with SiO_2, (b) the expectation that it may form a suitable barrier to preclude the oxidation of the underlying Ge and therefore the formation of the leaky and trap-filled Ge oxides, and (c) a prediction that the resultant epitaxial hetero-barrier might significantly enhance field-effect transistor (FET) performance, particularly the *p*-channel mobility/transconductance. A schematic illustrating the structure is shown in Figure 1. Such a structure exhibited significant advances over past accomplishments in terms of achieving an excellent electrical interface between SiO_2 and Ge. Capacitors formed with such a structure on both *n*- and *p*-Ge have shown[1] mid-gap interface state densities of 5×10^{10} cm^{-2} eV^{-1} and no hysteresis. This represents an approach to interface engineering wherein two materials with desirable properties (SiO_2, Ge) were brought together in a complex structure involving the use of a thin interlayer, in this case Si, to form a suitable *chemical* and electrical interface that would not have been realized otherwise. More importantly, such a concept has significant implications in the development of metal-insulator-semiconductor systems in a broad class of materials, especially those whose native oxides are unstable and detrimental to the formation of a good electrical interface. Several groups have achieved appreciable success in extending such a technology to materials systems based on GaAs[5-8], InGaAs[9-10], and InP[11]. Of

particular interest is the Ge_xSi_{1-x} materials system where appreciable success[12-14] has been demonstrated in applying such a concept to gate formation on Ge_xSi_{1-x}/Si heterostructures.

The key elements of this technology[1] are: (a) substrate surface cleaning for the removal of the detrimental native oxides, (b) deposition of an ultrathin, epitaxial Si interlayer on the clean semiconductor surface, and (c) deposition of the SiO_2 gate dielectric on the Si layer. We have demonstrated success in the application of this technology to MIS systems based on both Ge[1-4] and GaAs[5-6] by performing all of the above steps *in situ* and sequentially at low temperature (300°C) in a single-chamber *remote* plasma-enhanced chemical vapor deposition (RPECVD) system.

A crucial issue is to determine the role of the Si interlayer in the formation of the semiconductor-oxide interface. It is clear that the Si interlayer should possess an optimum thickness for suitable device operation, must completely cover the Ge surface, and must successfully preclude the oxidation of the underlying Ge during deposition of the SiO_2 overlayer (about 150 Å). The first issue, viz. the optimum thickness of the Si interlayer, is governed by two main constraints: the layer should be single-crystalline and defect free, and, for field-effect-transistor (FET) applications, it must be sufficiently thin so that interfacial strain can be controlled for band-gap engineering (e.g. type II heterostructures for n-channel confinement[15]). These issues are influenced significantly by the technology (particularly, the substrate temperature) involved in the Si and the SiO_2 depositions. The issue of *subcutaneous oxidation*[16,17] during SiO_2 deposition has direct bearing on the success of this technology. The subcutaneous

process[17], involving a consumption of the silicon due to oxidation, determines the amount of silicon at the interface and, therefore, the electrical properties[16] of the semiconductor-oxide interface. In fact, spectroscopic ellipsometric studies on similar insulator structures formed on GaAs showed little or no silicon remaining at the surface[7,18].

Two fundamental questions thus seem pertinent to the processing at hand: (1) What thickness of elemental silicon (if any) exists in its elemental form at the interface after the deposition of about 150 Å of the SiO_2 dielectric? (2) Is the underlying semiconductor (Ge) still unoxidized?

In the present study, we have used surface chemical analyses to address the above issues as they pertain to the formation of the structure on Ge by sequential processing in a single-chamber RPECVD system. Quantitative x-ray photoelectron spectroscopy (XPS) has been used to establish the degree of subcutaneous oxidation, the amount of unconsumed Si remaining at the interface, and the deposition rate at the initial stages of the oxide film growth.

Finally, we discuss some electrical results on MIS capacitors and field-effect-transistors (MISFETs) fabricated in Ge using this gate dielectric technology.

II. EXPERIMENTAL

The RPECVD reactor used for the fabrication of this structure is described elsewhere[19,20]. Following wet-chemical cleaning procedures[3,21], the Ge wafer was loaded immediately in the load-lock chamber and subsequently transferred to the main chamber of the RPECVD reactor. The *in situ* cleaning, the Si interlayer deposition, and the SiO_2 gate dielectric deposition were all performed at 300°C and sequentially in the same remote-plasma reactor. The *in situ* cleaning of the substrate surface was performed using hydrogen that was activated downstream from a remote Ar discharge[20,21]. The *in situ* cleaning treatment has been shown from Auger electron spectroscopy (AES) analyses to remove surface carbon and oxygen[21]. The concomitant formation of a reconstructed surface has been verified using reflection high energy electron difraction (RHEED) analyses[21]. The silicon layer was then deposited[22] by the downstream dissociation of SiH_4 using a remote Ar discharge. The Si deposition was performed at 300°C using low rate conditions: 200 sccm Ar and 5 sccm downstream SiH_4 (2% SiH_4 in He), a process pressure of 64 mTorr, and a 30W rf discharge for a duration of 5 min to deposit a layer about 25 Å thick (expected from deposition rate measurements on thicker layers). RHEED results have shown the silicon layer to be single-crystalline[3]. The SiO_2 overlayer was then deposited with a remote plasma process[23] at 300°C and a process pressure of 80 mTorr using a remote oxygen plasma (200 sccm, 20% O_2 in Ar) and the downstream introduction of SiH_4 (10 sccm, 2% SiH_4 in He). The SiO_2 deposition rate under these conditions was determined from step-height measurements on thick films and capacitance measurements on thin films. This rate is 8 Å/min. Structures without the Si interlayer were also prepared by a similar

in situ and sequential process to serve as a vehicle for comparison against the structures with the silicon interlayer.

Ion scattering spectroscopy (ISS) and x-ray photoelectron spectroscopy (XPS) were performed *ex situ* in a Leybold-Heraeus surface analytical unit by transferring the sample in air to the analytical chamber. For ISS analyses, a low-energy He^+ ion source (1500 eV) was employed. XPS analyses were performed using an Al-K_α radiation source ($h\nu$ = 1.486 keV). The angle of the entrance axis of the hemispherical analyzer in relation to the line perpendicular to the sample surface is 20°.

Depositions were interrupted at various stages and samples retrieved from the RPECVD reactor for *ex situ* analysis in the surface analytical unit.

Electrical evaluation of this gate dielectric technology was performed in separate experiments with MIS capacitors and *p*-channel inversion-mode MISFETs. Al was employed as the gate electrode material. The capacitor area was 5×10^{-4} cm^{-2}. The MISFETs were fabricated with boron-implanted source-drain regions, and employed a gate of length 2 μm and width 50 μm. A post-metallization anneal (400°C/30 min in N_2) was performed in both the capacitor and the FET fabrication sequences. No other processing at temperatures greater than 300°C is required following gate deposition.

III. RESULTS and DISCUSSIONS

A. Surface Analysis

(i) Ge Surface Coverage

One of the important roles expected of the Si is the preclusion of the oxidation of the underlying Ge surface. This requires complete coverage of the semiconductor surface by the Si overlayer. Figure 2 shows the ISS scan from a Ge sample with the ultrathin silicon layer deposited by the remote plasma technique following *in situ* cleaning of the Ge surface. The scan shows peaks attributable to Si and O with no detectable Ge, attesting to the complete coverage of the Ge surface by the silicon overlayer. Note that the Ge is revealed only after the Si layer was sputtered through with an Ar^+ ion beam. The oxygen is believed to have arisen due to the oxidation of the silicon during transfer of the sample in room air to the surface analytical unit.

(ii) Subcutaneous Oxidation And Its Effect On Si Interlayer Thickness

In a previous report[1], XPS analysis of the Ge-2*p* peak after about 20 Å deposition of Si has shown that the Ge surface remains virtually unoxidized despite the air transfer of the sample from the deposition chamber to the surface analytical unit. It must be mentioned, however, that the oxygen plasma during the subsequent RPECVD gate oxide deposition provides a harsh oxidizing environment that may potentially reduce the efficacy of the ultrathin Si layer to serve as a barrier to the oxidation of the underlying

semiconductor. In comparison with the room air environment, the oxygen discharge provides excited atomic, molecular, and ionic oxygen species which are highly reactive, and for the case of charged species, may demonstrate field-related diffusion effects that may potentially result in subcutaneous oxidation and therefore an appreciable consumption of the silicon interlayer. Note also that the pseudomorphic Si is in a strained state that can alter its oxidation rate compared to bulk silicon.

Figures 3(A) and (B) show high-resolution XPS spectra in the Si-2*p* and the Ge-3*d* energy windows from the sample after various stages of processing: (a) from a clean, bare Ge surface, (b) after a 5 min Si deposition for a layer of about 25 Å thickness (from deposition rate measurements) on a clean Ge surface, (c) after a 1.5 min oxide deposition on the Si layer under conditions discussed above to yield a layer about 12 Å thick (from deposition rate measurements), (d) after a second 1.5 min oxide deposition for an additional 12 Å oxide film, (e) after a third 1.5 min oxide deposition, and (f) after a fourth 15 min oxide deposition for an additional 120 Å oxide. Notice the attenuation of the Ge-3*d* (substrate) and the Si-2*p* (Si) peaks due to the increasing overlayer thicknesses. Note also the simultaneous increase in the Si-2*p* (SiO_2) signal.

The functional relationship between the attenuation of the peak intensity and the overlayer thickness is given by[24]

$$I_f = I_0 \exp\left(\frac{-t}{\lambda_n^m \operatorname{Cos} \theta}\right) \qquad \text{—Equation (1)}$$

where I_0 is the initial peak intensity, I_f is the final peak intensity, t is the thickness of the overlayer deposited, θ is the angle between the entrance axis of the hemisperical analyzer and a line perpendicular to the sample surface (20°), and λ_n^m is the inelastic mean free path or the escape depth of the photoelectrons from source material n in the overlayer of material m.

For quantitative analysis, the area of the peak was chosen as a measure of the photoelectron intensity. Spectral deconvolution was performed to extract the Ge-3d, Si-2p^{0+} (elemental Si) and the Si-2p^{4+} (SiO_2) peak intensities. Individual line shapes were simulated with a symmetric voigt shape (i.e. a Lorentzian convoluted with a Gaussian) using a least-squares fitting procedure. Background subtraction was performed using a non-linear function (Shirley function[25]) proportional to the integral of the elastically scattered particles. The Si-2p^{0+} (Si) peak was simulated[26] with a doublet constituted of the two spin-orbit components $2p_{1/2}$ and $2p_{3/2}$. The line shapes of these two peaklets (full-width-at-half-maximum, FWHM = 1.08 and 1.04 eV, respectively) were obtained by a fit of the Si-2p^{0+} line from a clean Si substrate while forcing a doublet separation of 0.6 eV and an intensity ratio, ($I_{2p}^{1/2}/I_{2p}^{3/2}$) of 0.5[27,28]. It must be noted that the peak shape of each intermediate oxidation state (Si^{1+}, Si^{2+}, and Si^{3+} -- viz. Si bonded to one, two, and three oxygen atoms respectively) is also a doublet of the two spin-orbit components. For this analysis, however, these are assumed to be lumped into a single symmetric line shape representing each oxidation state. The assigned peak position for the Si-2p^{1+} state was displaced from the Si-$2p_{3/2}^{0+}$ (Si) component by 1.0 eV as reported in literature[27,28]. The other two intermediate oxidation states (Si-2p^{2+}, and Si-2p^{3+}) were assigned positions at 100.05 and 100.8 eV. These are in close agreement with Hollinger and

Himpsel's observations[27,28]. A FWHM value of 1.0 eV was arbitrarily assigned to each intermediate oxidation state. The Si-$2p^{4+}$ (SiO_2) line shape (FWHM = 1.89 eV) was obtained from a thick oxide film. The peak shape of the Ge-3*d* line was obtained from a clean Ge substrate (FWHM = 1.5 eV). Note that the spin-orbit splitting of the Ge-$3d^{0+}$ peak was not accounted for since freedom from Ge oxidation required no further analysis of Ge oxidation states. For the quantitative analysis, the Si-$2p^{0+}$ line intensity was obtained from the sum of the line intensities of the individual spin-orbit components. The normalized line intensities for the respective peaks are shown in Table 1.

Table 1: XPS analysis of the Ge-3d and Si-2p signal intensities at various stages of processing

PROCESS STEP	NORMA--LIZED Ge-3d INTENSITY	NORMA--LIZED Si-2p (Si) INTENSITY	CONSUMED Si (Å)	SUBCUTA--NEOUS SiO_2 (Å)	DEPOSITED SiO_2 (Å)	TOTAL SiO_2 (Å)	TOTAL Si (Remaining) (Å)
Clean Ge	1.000	---	---	---	---	---	---
Si Deposition	0.273	1.000	---	---	---	---	28.0
First SiO_2	0.234	0.636	4.22	9.6	2.2	11.8	23.8
Second SiO_2	0.171	0.455	Nil	Nil	10.7	22.5	23.8
Third SiO_2	0.122	0.316	Nil	Nil	11.5	34.0	23.8
Fourth SiO_2	<<	<<	Nil	Nil	~120.0	154.0	23.8

A note on the above deconvolution procedures is appropriate at this point. The intermediate oxidation states are not resolved in the data. However, these features have been resolved and documented by other investigators[27,28]. The Si-2p^{0+} spin orbit doublet splitting and intensity ratio is also well established[24,28]. Additional factors such as hydrogen-related peak shifts[29] have been ignored. This information has been used in deconvolving the spectra so that *qualitative* trends in the distribution of oxidation states with thickness could be observed and compared with results from thermal SiO_2/Si interfaces. Clearly, uncertainties inherent in the approach will preclude the exact quantification of these (Si^{1+}, Si^{2+}, and Si^{3+}) features.

The inelastic mean free paths of the Si-2p photoelectrons in Si (λ^{si}_{si2p}) and SiO_2 (λ^{ox}_{si2p}) are taken to be 22 Å and 34 Å respectively[30,31]. Similar values for the Ge-3d photoelectrons, λ^{si}_{ge3d} and λ^{ox}_{ge3d}, are taken as 23 Å and 36 Å respectively. Note that considerable disagreement over these values exists in literature[32-35]. After the first Si deposition [spectra (b), Figure 3], the attenuation of the Ge-3d peak is entirely from the Si overlayer due to the negligible formation of a native oxide during the air transfer as is evident from the spectra. From the Ge-3d peak intensity before and after the Si deposition, therefore, we obtain the Si layer thickess to be 28 Å which agrees very well with the thickness expected from the Si deposition rate (25 Å).

Following the first oxide deposition, we observe distinct Si-2p peaks from both the SiO_2 overlayer (Si^{4+} oxidation state, binding energy, BE ~ 103 eV) and the elemental silicon (Si^{0+} oxidation state, BE ~ 99 eV) interlayer [spectra (c), Figure 3]. This of course establishes that the elemental silicon

interlayer is still present after the first oxide deposition. As can be expected, we also observe the attenuation of *both* the Ge-3*d* and the Si-2p^{0+} (elemental Si) peaks. A simple application of equation 1 on the Ge-3*d* peak intensities yields an oxide overlayer thickness of 5.2 Å. *If there were no subcutaneous oxidation,* this value would then represent the thickness of the deposited oxide. A similar application of the above relationship on the Si-2p^{0+} (Si) peak intensities, however, yields the oxide overlayer thickness to be 14.4 Å. The disparity in these numbers and especially the high number derived from the Si-2p^{0+} (Si) analysis suggests a disproportionate decrease in the Si-2p^{0+} intensity after the first oxide deposition. This can be explained as due to the partial consumption of the Si interlayer from subcutaneous oxidation during the oxide overlayer deposition.

An analysis of the peak intensities to account for subcutaneous oxidation and the amount of Si consumed is done in the following manner. Figure 4 summarizes the phenomenon believed to occur during the first oxide deposition. It is commonly held that direct oxidation of the silicon surface results in forming an oxide layer which is nominally 2.27 times the thickness of the consumed silicon[36,37]. Thus, if x is the thickness of the silicon layer (initially 28 Å) consumed, then the thickness of the remaining silicon layer is $(28 - x)$ and that of the oxide is $(t_{dl} + 2.27x)$ where t_{dl} is the thickness of the SiO_2 deposited. The Ge-3*d* intensity is attenuated both due to the silicon and the oxide overlayers. The attenuation of the Ge-3*d* peak intensity can therefore be written as

$$I_{ge,1} = I_{ge,o} \exp\left[\frac{-(t_{dl} + 2.27x)}{\lambda^{ox}_{ge3d}\,\mathrm{Cos}\,\theta} + \frac{-(28 - x)}{\lambda^{si}_{ge3d}\,\mathrm{Cos}\,\theta}\right] \qquad \text{— Equation (2)}$$

The Si-$2p^{0+}$ (Si) peak intensity, however, is reduced due to two factors: (i) the overlayer oxide thickness, and (ii) a *decrease* in the Si thickness due to its partial consumption. Note that the thickness of the Si is on the order of the escape depth of the photoelectrons. Any changes in the thickness will affect the excited volume and therefore the source intensity, unlike the case for the Ge-3*d* peak. In order to apply equation 1 to the Si-$2p^{0+}$ intensity, we must estimate the source intensity by accounting for Si consumption due to subcutaneous oxidation.

The line intensity, I_f^y, from a film of material f with an effective thickness y can be expressed in terms of the intensity I_f^∞ from the pure bulk material. This relationship, derived using equation 1, is expressed in the following way:

$$I_f^y = I_f^\infty \left[1 - \exp\left(\frac{-y}{\lambda_f^f \operatorname{Cos}\theta}\right) \right] \qquad \text{— Equation (3)}$$

Thus, the source intensity from the remaining silicon after the first oxide deposition step, $I_{si}^{(28-x)}$, can be expressed in terms of the intensity $I_{si,o} = I_{si}^{28}$ of the initial 28 Å Si layer which is known. Note that this is now attenuated by the oxide overlayer. The resulting intensity of the Si-$2p^{0+}$ (Si) peak after the first oxide deposition, therefore, can be written as

$$I_{si,1} = I_{si,o} \frac{\left[1 - \exp\dfrac{-(28 - x)}{\lambda_{si2p}^{si} \operatorname{Cos}\theta} \right]}{\left[1 - \exp\dfrac{-28}{\lambda_{si2p}^{si} \operatorname{Cos}\theta} \right]} \exp\left[\frac{-(t_{d1} + 2.27x)}{\lambda_{si2p}^{ox} \operatorname{Cos}\theta}\right] \qquad \text{— Equation (4)}$$

Equations 2 and 4 can then be solved simultaneously to yield the amount of Si consumed x = 4.2 Å, the thickness of deposited oxide t_{d1} = 2.2 Å, the total thickness of the oxide over silicon t_{d1} + $2.27x$ = 11.8 Å, and the amount of Si remaining unconsumed = 23.8 Å, after the first oxide deposition. These results are shown in Table 1.

While we have established the occurence and extent of subcutaneous oxidation and consequent consumption of Si during the first 10 Å deposition of the SiO_2 film, a question arises: is the subcutaneous oxidation a *continuous* phenomenon as the SiO_2 deposition proceeds? An answer was obtained by analysis of the Ge-3*d* and the Si-$2p^{0+}$ (Si) intensities after yet another 10 Å oxide deposition. Figure 3 [spectra (d)] shows the XPS spectra after the second 1.5 min oxide deposition. Notice again that we observe distinct Si-2*p* peaks from the Si and the SiO_2 attesting that the elemental Si survives through the deposition of a total oxide of about 20 Å. If we assume that there was no further subcutaneous oxidation after the first oxide deposition, the attenuation of the Ge-3*d* peak is then due to the Si interlayer (now 23.8 Å) and the composite oxide ($11.8+ t_{d2}$) where t_{d2} is the thickness of the oxide deposited during the second step. On the other hand, the attenuation of the Si-$2p^{0+}$ (Si) peak (source intensity from remaining silicon = $I_{si}^{23.8}$) is due to the ($11.8+ t_{d2}$) oxide. The respective relationships for the Ge-3*d* and the Si-$2p^{0+}$ intensities can then be written as:

$$I_{ge,2} = I_{ge,o} \exp\left[\frac{-(11.8 + t_{d2})}{\lambda^{ox}_{ge3d} \operatorname{Cos}\theta} + \frac{-23.8}{\lambda^{si}_{ge3d} \operatorname{Cos}\theta}\right] = I_{ge,1} \exp\left[\frac{-t_{d2}}{\lambda^{ox}_{ge3d} \operatorname{Cos}\theta}\right]$$

— Equation (5)

$$I_{si,2} = I_{si}^{23.8} \exp\left[\frac{-(11.8 + t_{d2})}{\lambda_{si2p}^{ox} \text{Cos } \theta}\right] = I_{si,1} \exp\left[\frac{-t_{d2}}{\lambda_{si2p}^{ox} \text{Cos } \theta}\right] \quad \text{—Equation (6)}$$

The thickness of the second deposited oxide, t_{d2}, is thus obtained to be 10.65 Å from equation (5) or 10.75 Å from equation (6).

The analyses of the Ge-3*d* and the Si-$2p^{0+}$ (Si) intensities after the second oxide deposition thus yield comparable numbers for the second deposited oxide thickness to within 5%. The assumption that *there is no further subcutaneous oxidation* during the second oxide deposition sequence is therefore valid within the sensitivity of this data.

A similar analysis of the Ge-3*d* and the Si-$2p^{0+}$ (Si) intensities after the *third* oxide deposition [spectra (e), Figure 3] again yields comparable numbers (11.4 and 11.6 Å respectively) for the third deposited oxide thickness, confirming that that there is no further subcutaneous oxidation. These and the preceeding results are summarized in Table 1.

Note that the preceeding analysis has been based on the Ge-3*d* and the Si-$2p^{0+}$ (Si) peaks. Notice that the Si-$2p^{4+}$ (SiO_2) feature increases in intensity as the oxide deposition proceeds until it virtually saturates when a thick oxide (150 Å) is formed. The numerical values derived for the oxide thicknesses in the earlier analysis can be checked for consistency with numbers derived from the Si-$2p^{4+}$ (SiO_2) intensities (using equation 3). In fact, excellent agreement is observed in all cases except the first oxide deposition step where a higher value (~17 Å) is predicted from the initial Si-$2p^{4+}$ intensity. Several different factors were considered in an attempt to

explain this discrepancy. One possibilility is that the interfacial Si^{4+} oxide, formed largely by the consumption of Si, is denser than a conventional SiO_2 and therefore a higher number density of Si atoms could yield a higher Si-$2p^{4+}$ intensity. A second factor is that the interfacial oxide can have an inelastic mean free path less than that found in bulk oxides. This can arise both as a result of a higher Si^{4+} density and due to a strained region arising out of a lattice mismatch as pointed out by Vasquez and Grunthaner[38] in studies of thermal oxides. A third factor can be clustering/islanding of the oxide during the first stages of growth, in which case the Si-$2p^{4+}$ (oxide) intensity is more or less unaffected while the Si-$2p^{0+}$ (Si) and the Ge-3*d* photoelectrons suffer *less* attenuation thus predicting a lower overlayer thickness. A fourth plausible explanation is suggested in the following manner. The earlier analysis of the Ge-3*d* and the Si-$2p^{0+}$ (Si) intensities assumes a homogeneous mixture of all the oxidation states in the first oxide. It is more likely, however, that the first oxide is of a *non-homogeneous composition*, viz. a homogeneous Si^{4+} (SiO_2) film formed over a layer composed of the intermediate oxidation states. This rearrangement will not influence the attenuation of the Si-$2p^{0+}$ (Si) and the Ge-3*d* signatures. However, the Si-$2p^{4+}$ signature will now appear more intense. A fifth factor that comes to mind is the possibility of a different conversion factor (other than 2.27) for the oxide thickness due to the consumed silicon. The first of the factors discussed above can be evaluated only with an understanding of the relative densities of the plasma oxide and a conventional oxide *near the interface* and is not attempted in this work. The last factor, viz. a different conversion factor for the oxide thickness due to the consumed Si, simply changes the relative thicknesses of the plasma oxide and the deposited oxide but does not alter the *total* thickness of the first oxide[37]. The other three

factors were simulated with simple models that were superimposed on the earlier equations. It was observed that all of the effects were in the right direction. The second issue, viz. lower escape depth, had a stronger influence relative to the other two; yet, none of these could individually explain the observed inconsistency. More detailed analysis of the data however depends on interfacial parameters not known at the present time. A comprehensive model may offer a consistent solution with numbers that are slightly different from the ones derived earlier, but will not alter the general conclusions of this work.

We have established thus far that we detect no further subcutaneous oxidation/consumption of the silicon following the formation of the initial few layers of the oxide. It is however important to establish the extent of this phenomenon when SiO_2 layers on the order of 150 Å are deposited, as employed in nominal device structures[1-11]. Further XPS analysis, however, is severely impeded by the fact that the escape depth of the photoelectrons in the respective materials allows analysis of only thin overlayers that are no more than about three times its value in thickness. One approach to circumvent this problem is to analyze the sample after selective wet-chemical etching of the oxide. After the deposition of an additional ~120 Å SiO_2 (total 150 Å, as in a nominal device[1]), the oxide was removed by etching in buffered HF solution followed by a deionized water rinse/air transfer. Figure 5 shows the XPS spectra in the Si-2*p* and the Ge-3*d* windows from the sample surface after the oxide removal step. The distinct appearance of the Si-$2p^{0+}$ (Si) peak clearly establishes the presence of elemental Si at the surface. The slight shoulder on the peak was verified from glancing angle analysis to be that from a surface oxide that was presumably left behind due to incomplete

etching of the oxide and/or reoxidation of the silicon interlayer surface during the subsequent deionized water rinse and air transfer to the surface analytical unit. Notice that the smaller Si-2*p* peak [Fig. 5A(a) versus Fig. 5A(b)] and the larger Ge-3*d* peak [Fig. 5B(a) versus Fig. 5B(b)] is a consequence of silicon consumption. The Ge-3*d* intensities suggest that there is at least an 18 Å thick layer of elemental Si at the interface. This number is clearly not in agreement with 23.8 Å derived from the consecutive 10 Å deposition sequences. This disagreement cannot be merely attributed to subcutaneous oxidation during the final 120 Å oxide deposition due to (i) uncertainties in the selectivity of the etching process and its dependence on strain in the pseudomorphic layer, and (ii) reoxidation effects from ambient exposure as can be seen in Fig. 5B(a).

In summary, we observe that the Si interlayer is largely preserved through the deposition of the entire ~150 Å SiO_2 deposition. During the first oxide deposition, the phenomenon of subcutaneous oxidation consumes a little over 4 Å of the starting 28 Å of the Si interlayer during the first stages of growth. The oxide formed (11.8 Å) is constituted predominantly of the subcutaneous oxide (9.6 Å) along with a small component due to the deposited oxide (2.2 Å) . The second and the third deposition sequences, performed under the same conditions as the first deposition sequence, result in oxide thicknesses of 10.7 Å and 11.5 Å respectively. No oxidation/consumption of the Si is observed in these subsequent stages of film formation, and the oxide formed is entirely a result of the deposition process. These observations thus lead us to believe that *the subcutaneous oxidation or consumption of the Si is mostly a result of the plasma oxidation of the silicon during the initial stages of the RPECVD SiO_2 deposition.*

Furthermore, the phenomenon is greatly limited (if not terminated) after the formation of the first few layers of SiO_2; the oxide thus presumably serving as a barrier to the diffusion of oxygen species which can be expected to be negligible at the operating temperatures (300°C) and oxygen partial pressures (15 mTorr) of the RPECVD deposition. We note that the oxide thickness deposited on the Si interlayer is consistently less than that deposited on subsequent oxide surfaces under the same conditions. Another significant observation is that the silicon is seen in its elemental form at the Ge surface following the formation of an oxide of total 150 Å over the Si interlayer and its subsequent selective removal by etching in HF.

(iii) Preclusion of Oxidation of Ge Surface

It is important to recognize that the Si interlayer plays a crucial role in preserving the clean Ge surface by precluding the formation of the detrimental Ge-oxides. The Ge-3*d* spectra in Fig. 3 at various process steps show the conspicuous absence of Ge-oxides (BE ~ 29-32 eV) through all processing. This is in contrast to the case where SiO_2 is directly deposited on Ge which reveals [Fig. 6(a)] a shoulder on the Ge-3*d* peak that is indicative of the presence of various oxidation states[39] (Ge^{1+}, Ge^{2+}, Ge^{3+}, and Ge^{4+}) at the SiO_2/Ge interface. Figure 6(b) shows the Ge-3*d* spectrum after the ~150 Å composite SiO_2 is etched off from the sample. The absence of any Ge-oxide features (while SiO_x features are present, as seen in Fig. 5) suggests that the Ge surface *still remains* protected from any oxidation. The ultrathin Si interlayer thus provides complete coverage and protects the Ge surface from native oxidation even in an aqueous ambient (deionized water rinse), which presents a more severe oxidation environment than air transfer, attesting to

its excellent coverage of the Ge surface. The formation of such a structure by *in situ* processing in a single RPECVD chamber integrating several different process steps through which the Si interlayer is largely preserved is a significant advantage of the remote-plasma enhanced CVD process.

In the context of the present findings, it must be reiterated that other groups[7,18] have observed little or no silicon remaining at the interface (from spectroscopic ellipsometric measurements) when similar concepts were employed in the formation of MIS structures on GaAs.

(iv) SiO_2/Si Interface Formation

Aside from gaining insight into the subcutaneous oxidation process and establishing the existence of the Si interlayer and its protection of the Ge surface from oxidation, several additional inferences can be made that have significant fundamental implications in the formation of the SiO_2-Si interface during RPECVD (and qualitatively for other plasma assisted processes) deposition of the gate oxide (for the conditions stated): (a) the true SiO_2-Si interface is actually between the semiconductor Si and the *plasma oxidized Si* rather than the deposited SiO_2, (b) that the SiO_2-Si interface is actually a *buried* interface about 4 Å beneath the starting Si surface, (c) surprisingly, the oxide thickness deposited on the Si interlayer is significantly less than the oxide thickness deposited on subsequent oxide surfaces (e.g. 2.2 Å versus 10.7 Å and 11.5 Å) for identical deposition parameters targeting a nominal thickness of about 12 Å. This phenomenon is not understood at the present time, and further studies are underway to arrive at an explanation, (d) while the first interfacial oxide is largely

composed of the Si^{4+} state, the plasma oxidation is nevertheless accompanied by the formation of intermediate oxidation states as is evident by the distinct increase in the relative intensity (with respect to Si^{0+}) of the Si^{1+} and the Si^{2+} components [see Figure 3(c)], (e) it is interesting to note that the Si^{1+} and the Si^{2+} components show maximum relative intensities after the first [Fig. 3(c)] and second oxide [Fig. 3(d)] deposition sequences respectively. This therefore suggests somewhat of a *layering* of these intermediate oxidation states with the Si^{1+} component being closest to the SiO_2/Si interface, (f) additionally, a higher proportion of the Si^{1+} and the Si^{2+} components relative to Si^{3+} state is observed in the first oxide. This contrasts with the observation of more or less uniform proportions of each of these states in a thermal oxide of comparable thickness[27], and (g) furthermore, it was shown[31] that during thermal oxidation the Si-$2p^{4+}$ (SiO_2) peak displacement from Si-$2p^{0+}$ (Si), δ , increases from 3.9 eV at the interface to about 4.4 eV at a distance of 60 Å into the bulk. Such an observation has been explained as due to a "near-interface" stoichiometric SiO_2 region that is strained and structurally distinct[30,40,41] from the bulk SiO_2. This has been argued[31,40] on the basis of a strain-induced charge transfer (SICT) model in which changes in the Si-O-Si bridging bond angle cause variation in the Si-to-O charge transfer and rehybridization effects[31]. We find from Figure 7(a) a similar transition region where δ increases from 4.05 eV at the interface (first oxide) to 4.5 eV at about 45 Å in the bulk. The range of this effect, viz. 35+ Å , is thus *significantly greater* than the thickness of the oxide component resulting from direct oxidation of the silicon, extending well into the deposited oxide. Given the low thermal budget processing (300 °C/25 min), this result was unexpected. Figure 7(b) shows the binding energy difference between the O-1*s* and the Si-$2p^{0+}$ (Si) signals. Note that the O-1*s* and Si-$2p^{4+}$ levels shift in the same

direction towards higher binding energies by slightly differing amounts and is consistent with data reported in literature[30,31].

B. Electrical Characterization

We must recognize that aside from precluding the formation of the detrimental Ge-oxides at the interface, the silicon interlayer forms a device quality electrical interface[1] with the underlying Ge. An example is shown in Figure 8 in the form of excellent capacitance-voltage (C-V) characteristics derived from a capacitor formed with such a composite dielectric on *n*-Ge. The mid-gap interface state density is obtained to be 5×10^{10} cm^{-2} eV^{-1}.

Characteristics of Ge MISFETS fabricated with the composite SiO_2-Si dielectric are shown in Figure 9. The figure shows the drain-current (I_d) versus drain-voltage (V_d) characteristics derived for different gate bias (V_g) values. The maximum room temperature *p*-channel transconductance (g_m) obtained from these characteristics is 52 mS mm^{-1} at a gate length of 2 μm. The peak effective channel hole mobility (μ_{eff}) determined from the measurement of the drain conductance at low drain voltages (-0.05 V) is 430 cm^2 V^{-1} s^{-1}. Negligible fixed-charge induced threshold shift is observed. In addition to lending the benefits of a low interface trap density, the pseudomorphic Si can be engineered to provide confinement of the conductive channel in a Si_xGe_{1-x} or Ge-based FET heterostructures. This exploits the advantages of the higher carrier mobilities in Ge or SiGe alloys, particularly hole mobilities. It is seen from the C-V analysis of the SiO_2-Si-Ge structure

that the accumulation capacitance is greater than the quasi-static capacitance for *n*-Ge (Figure 8), and vice versa for *p*-Ge[1]. Such an observation is explained on the basis of a hole barrier due to the valence band offset at the *n*Si-*n*Ge interface, in which case the Si would behave more like an insulator when the *n*-Ge is in inversion. In an enhancement-mode *p*-channel FET, thus, the hole transport can be confined in the Ge when the *n*-Ge is in inversion.

It must be remembered, however, that the Si interlayer thickness must be kept as small as possible and within the critical thickness limit for single-crystallinity. Dislocations at the interface will not only increase the interface state density but will also result in enhanced scattering of carriers leading to reduced channel mobilities. A strain-field in the epitaxial (pseudomorphic) layer is essential since it is conducive to increasing the effective barrier height for confinement of carriers and in lifting the heavy-hole/light-hole degeneracy. Additionally, a non-abrupt interface and higher Si interlayer thickness may cause the parasitic Si channel to dominate the channel transconductance during turn-on of the device as is observed by several groups[12,14]. Complete coverage at lower thicknesses can be a technology dependent issue. The remote-plasma deposited ultrathin (~20 Å), epitaxial Si layers have shown complete coverage and the capability to preclude oxidation of the underlying Ge during the subsequent deposition of the SiO_2 dielectric.

IV. CONCLUSIONS

We have examined the role of the ultrathin Si interlayer in the SiO_2-Si-Ge heterostructure. Ion scattering spectroscopy (ISS) has shown that the silicon layer offers complete coverage of the Ge surface prior to the deposition of the oxide dielectric. X-ray photoelectron spectroscopy (XPS) shows that the Si interlayer is largely preserved even after the deposition of 150 Å SiO_2. It is also observed that the Ge surface remains unoxidized. The Si interlayer forms excellent electrical interfaces with both SiO_2 and Ge, as attested by the observation of greatly reduced interface state densities (5×10^{10} cm^{-2} eV^{-1}). It can be engineered to confine channel transport in the Ge. A maximum room-temperature transconductance of 52 mS mm^{-1} and a peak effective channel mobility of 430 cm^2 V^{-1} s^{-1} has been obtained in an inversion-mode *p*-channel Ge MISFET (2 μm gate length) fabricated with the composite SiO_2-Si dielectric. XPS analyses at various stages of the SiO_2 deposition sequence have shown that (a) about 4 Å of the (28 Å starting) Si layer are consumed due to subcutaneous oxidation, (b) it seems that the Si consumption is a result of plasma oxidation of the Si layer from exposure to the oxygen plasma at the initiation of the discharge, and not by a gradual oxidation during the film deposition process. Subcutaneous oxidation is prevented thereafter by the formation of the initial few layers of the oxide which presumably act as a barrier to the diffusion of oxygen species, (c) the Si layer precludes the oxidation of the underlying Ge *through* the entire deposition of the 150 Å SiO_2 dielectric, (d) the SiO_2-Si interface is *buried* about 4 Å beneath the starting Si surface, (e) the true SiO_2-Si interface is formed between the semiconductor and the plasma-oxidized Si rather than the deposited SiO_2, (f) this plasma-oxidized Si is composed largely of stoichiometric oxide (Si^{4+}

oxidation state, SiO_2) whose formation is accompanied by formation of lower oxidation states (Si^{x+}; x = 1, 2, and 3) near the interface, (g) we have repeatedly found that the oxide thickness (first layer) deposited on the Si interlayer is significantly less than that deposited on the subsequent oxide surfaces (e.g. 2.2 Å versus 10.7 Å) under the same deposition conditions, and (h) the (Si-$2p^{4+}$ - Si-$2p^{0+}$) binding energy shift gradually increases from 4.05 eV at near-interface to about 4.5 eV in the bulk much like that observed at a thermal oxide-Si interface; the transition region (35+ Å) extending well beyond the thickness of the plasma-oxide (formed from the Si consumption) into the deposited oxide. The last five observations highlight important characteristics of SiO_2-Si interface formation with a plasma deposited SiO_2 dielectric film. All processing is performed at low temperature (300°C) using remote plasma-enhanced chemical vapor deposition (RPECVD). Sequential and *in situ* remote plasma processing is believed to be crucial in preserving the Si interlayer and the abrupt interfaces. This work demonstrates that high quality electrical interfaces (SiO_2/Si) can be formed with minimal consumption of Si. This can be important in the fabrication of Si-based heterostructure devices such as the heterojunction bipolar transistor[42], (emitter/base junction passivation) or the modulation-doped FET[43] (gating of strain-engineered structures).

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37. Note that the 2.27 value for the conversion factor for the oxide thickness due to consumed silicon is unlikely to be correct in the near-interfacial region where a mix of intermediate oxidation states, strain, and variations in ring structure will alter the value. We have allowed the value to vary in our model for quantitative analysis. A change in this value does not alter the amount of Si consumed or the total oxide thickness but slightly alters the relative amounts of the subcutaneous oxide and the deposited oxide. The general conclusions of this work thus remain unaltered.

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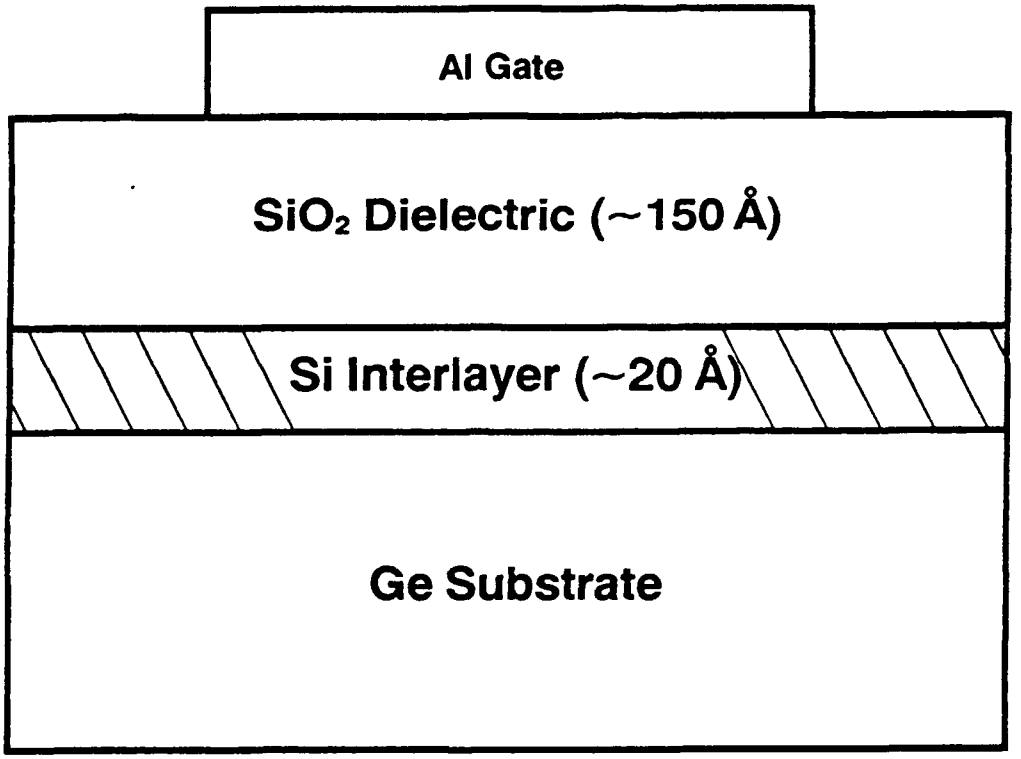

Figure 1 Interface engineering with pseudomorphic interlayers. An ultrathin (~20 Å) Si interlayer interposed between the semiconductor and the gate dielectric yields significant improvements to the electrical properties of the interface.

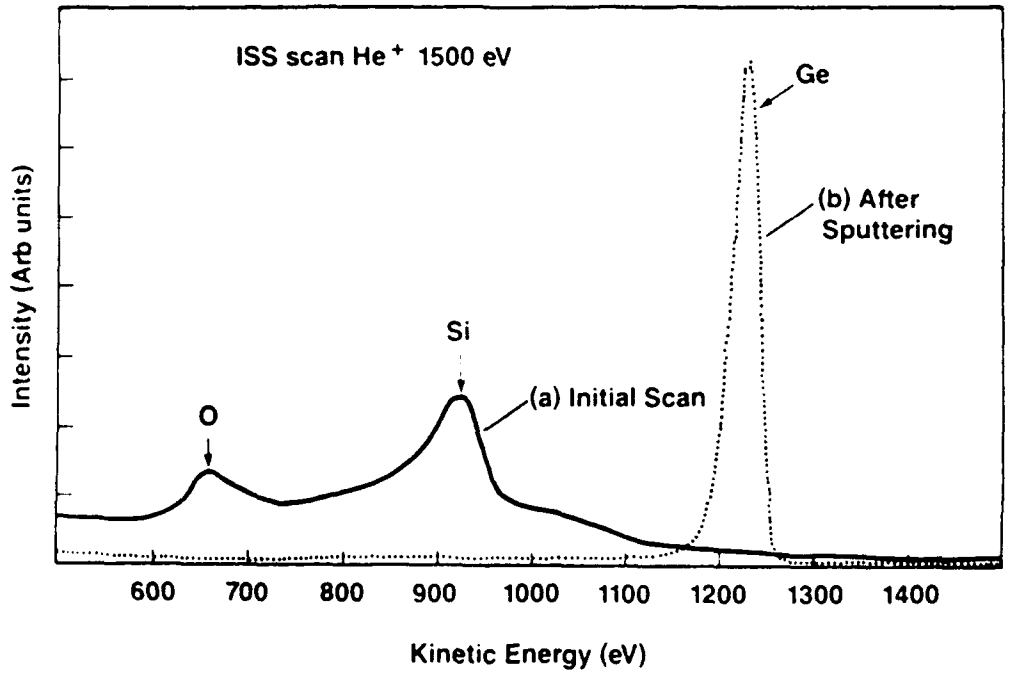

Figure 2 Low energy ISS analysis of the Ge surface (a) following a Si deposition. Note the conspicous absence of the Ge signature. The oxygen signal is believed to arise from a native oxide formed during the room-air transfer to the surface analytical unit, and (b) a similar spectrum from the same sample after Ar^+ sputtering that reveals the underlying Ge.

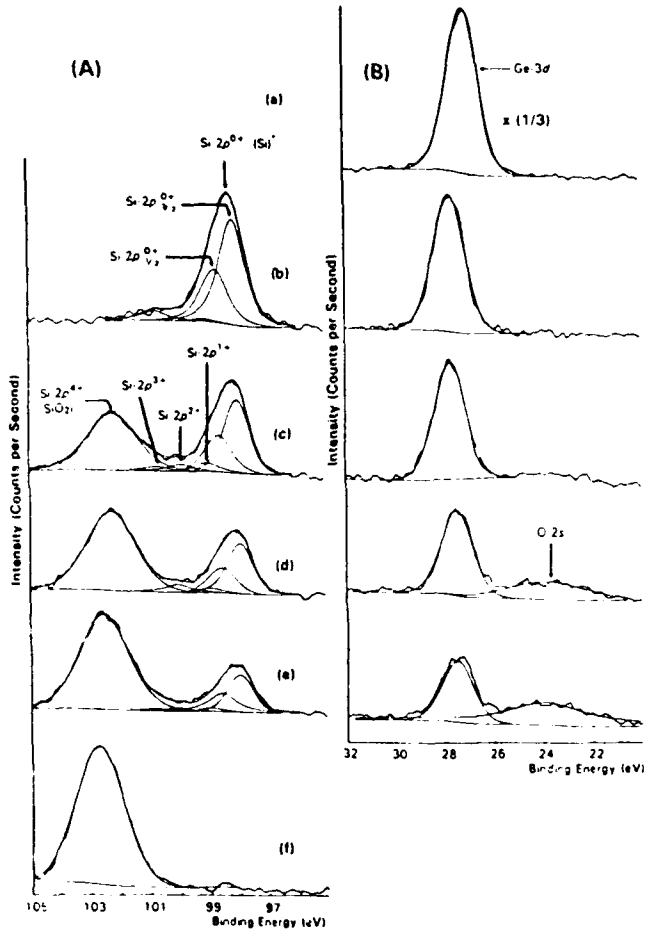

Figure 3 XPS spectra obtained in (A) Si-2*p* and (B) Ge-3*d* windows: (a) from a clean Ge surface, (b) after 5 min silicon deposition on a clean Ge surface, (c) a 1.5 min oxide deposition on the silicon, (d) after a second 1.5 min oxide deposition, (e) after a third 1.5 min oxide deposition, (f) after a fourth 15 min thick oxide deposition. The spectra are drawn to scale (except where reduction is indicated by a multiplication factor). Figures 3A(a) and 3B(f) have been ommitted because the Si-2*p* and Ge-3*d* signatures are absent in the respective stages of the process. All layers were deposited at low temperature (300°C) by the remote-plasma technique. Spectral decomposition has been performed on the acquired data which is indicated (smoothed) by the thin lines. Notice that the Ge surface remains protected from oxidation through all processing steps.

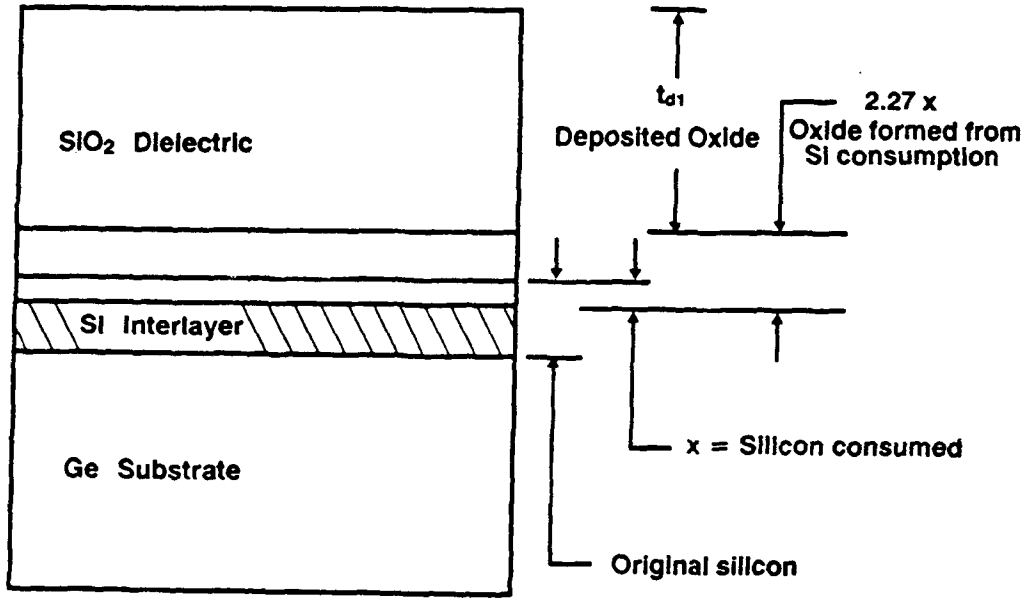

Figure 4 Schematic illustrating the phenomena after the deposition of the first oxide layer. The consumption of x Å of Si due to subcutaneous oxidation results in the formation of $2.27x$ Å of SiO_2[34]. The total oxide over the silicon therefore is $(t_{d1} + 2.27x)$ Å where t_{d1} is the deposited oxide thickness.

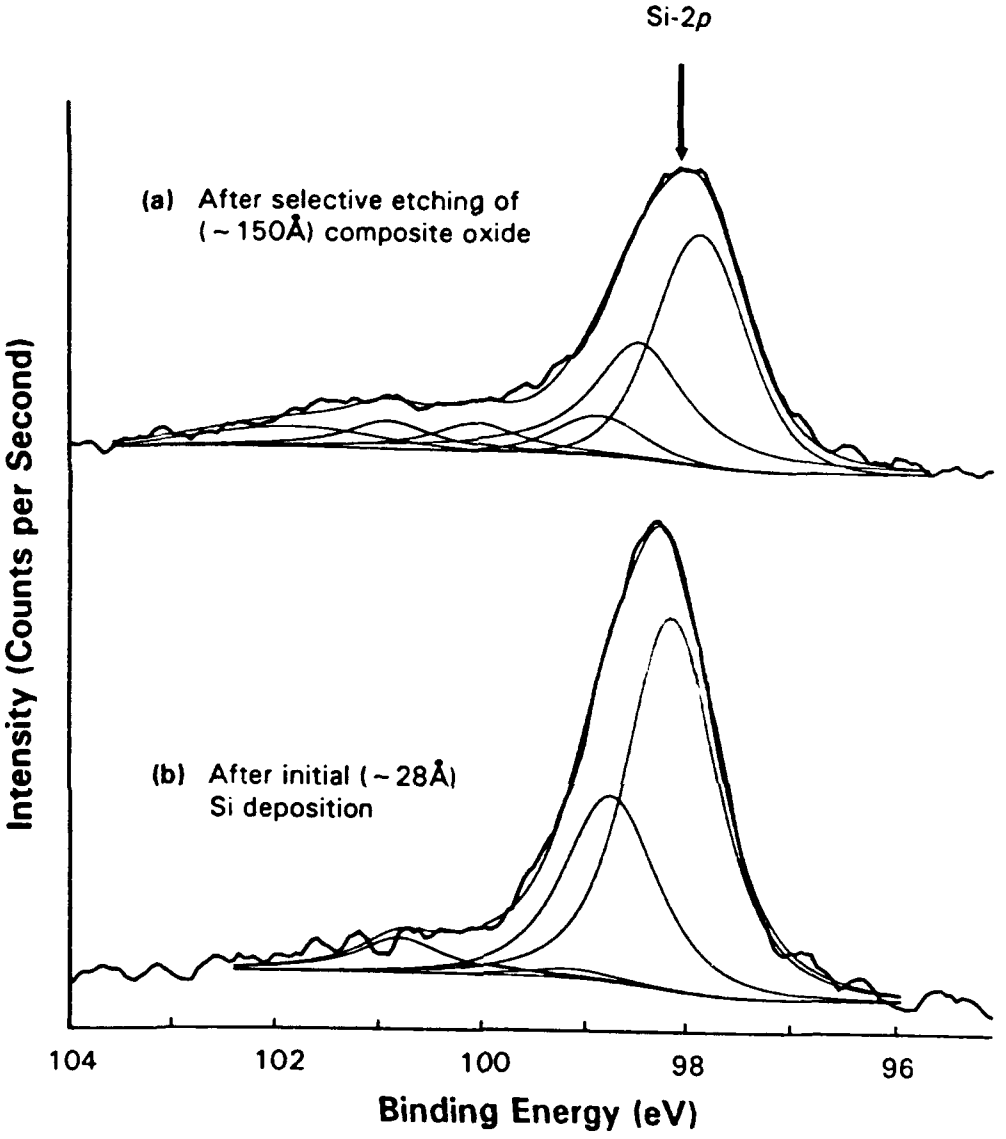

Figure 5 XPS analysis in the (A) Si-2*p* and (B) Ge-3*d* regions: (a) after etching the 150 Å composite oxide in a buffered-HF solution followed by a deionized water rinse, that reveals the presence of the Si interlayer, and (b) after the initial silicon (~28 Å) deposition. The spectra in each case are drawn to scale. Notice following the removal of the oxide that while silicon oxides are present the Ge surface still remains precluded from oxidation.

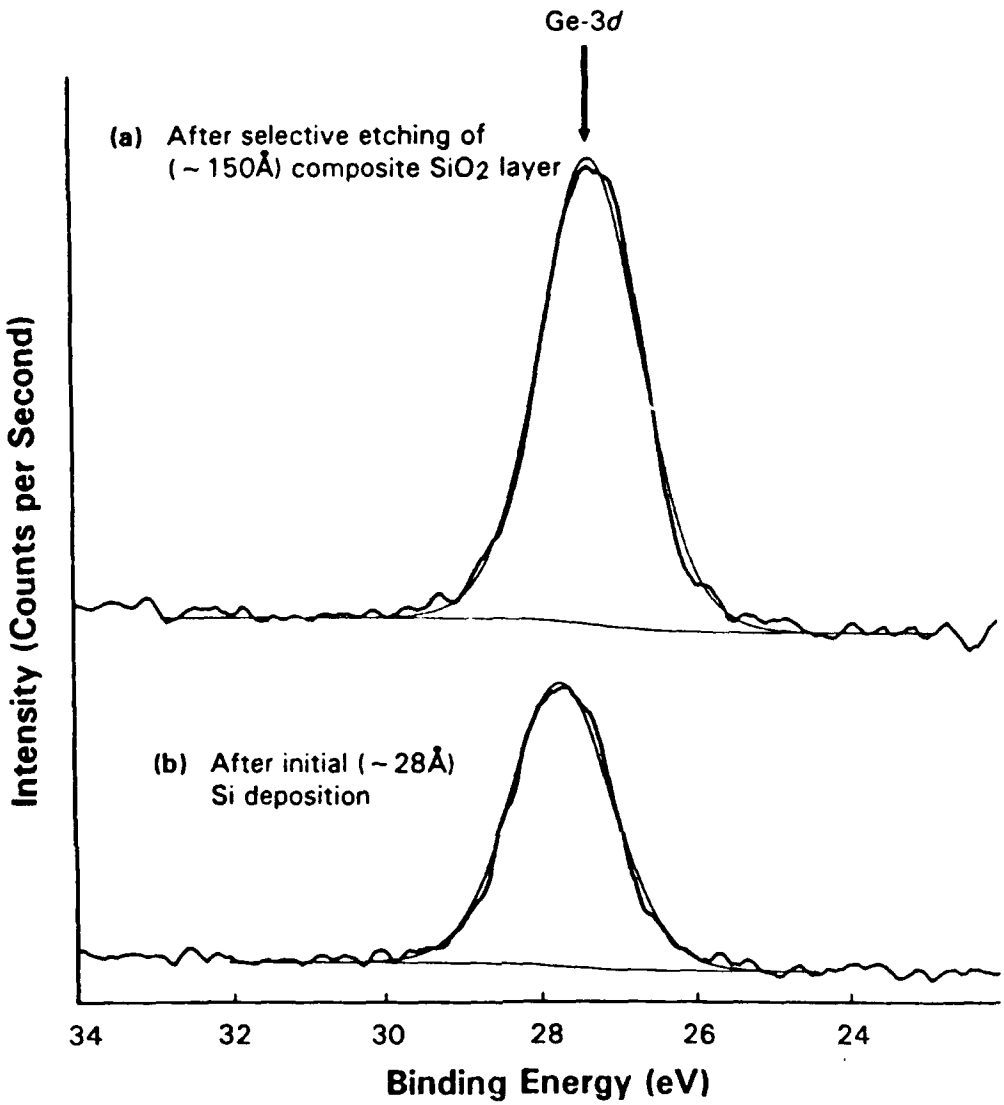

Figure 5 XPS analysis in the (A) Si-2*p* and (B) Ge-3*d* regions: (a) after etching the 150 Å composite oxide in a buffered-HF solution followed by a deionized water rinse, that reveals the presence of the Si interlayer, and (b) after the initial silicon (~28 Å) deposition. The spectra in each case are drawn to scale. Notice following the removal of the oxide that while silicon oxides are present the Ge surface still remains precluded from oxidation.

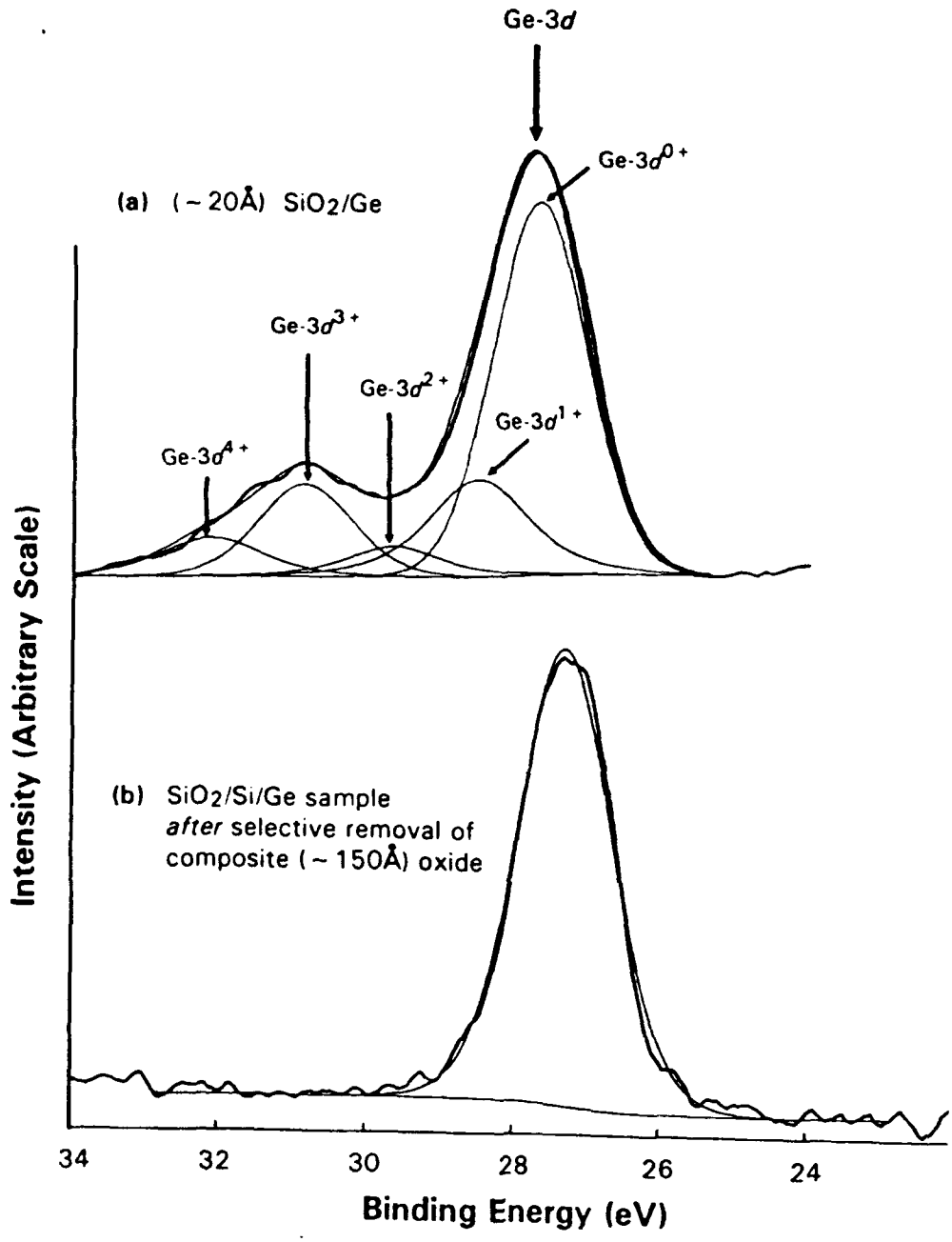

Figure 6 XPS analysis of the Ge-3*d* signature from (a) a (~20 Å) SiO_2/Ge sample where the RPECVD SiO_2 was deposited directly on the Ge substrate thus showing the presence of the detrimental Ge-oxides at the interface, and (b) the SiO_2/Si/Ge sample *after* removal of the composite 150 Å SiO_2 overlayer in buffered-HF followed by a deionized water rinse, where the Ge surface remains protected from oxidation by the Si layer.

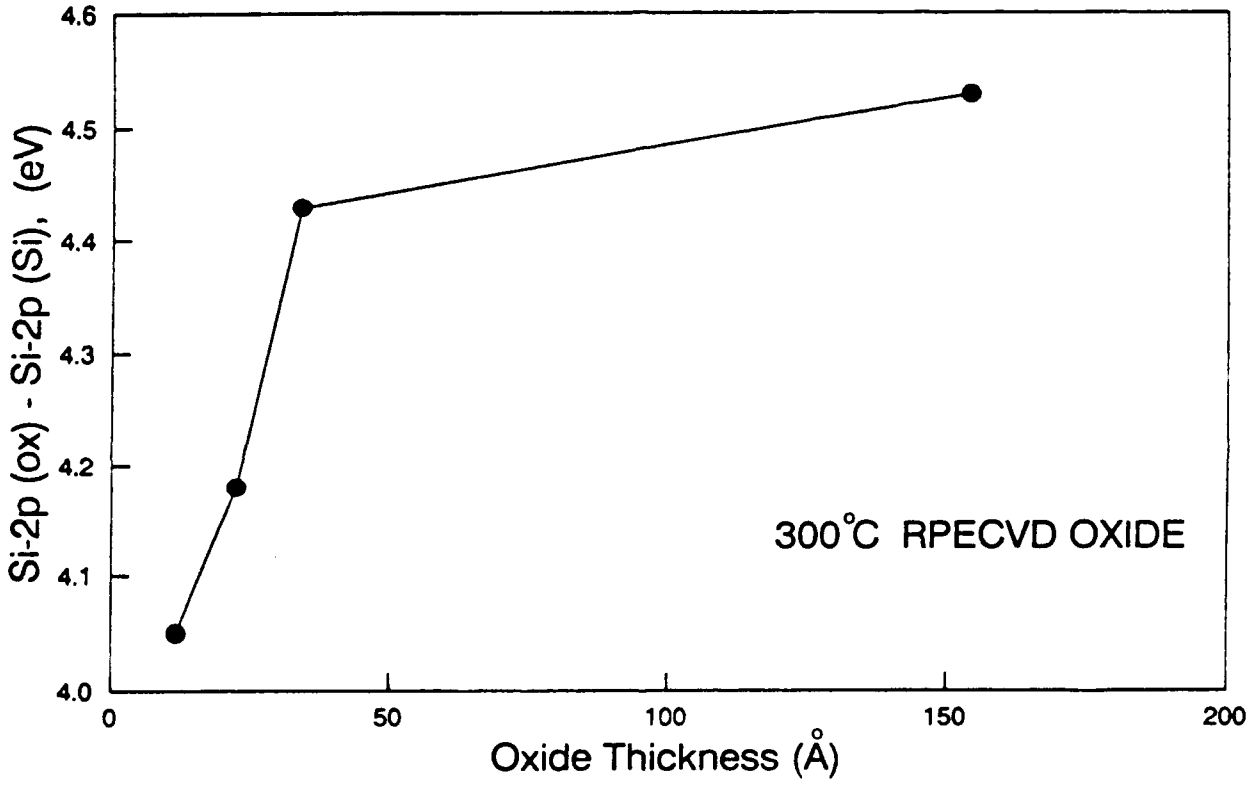

Figure 7 Binding energy differences as a function of oxide thickness from the interface: (a) between Si-2*p* (SiO_2) and the Si-2*p* (Si) signals, and (b) between O-1*s* and the Si-2*p* (Si) signals. The Si-2*p* (Si) position is taken to be that of the composite peak including both spin orbit components.

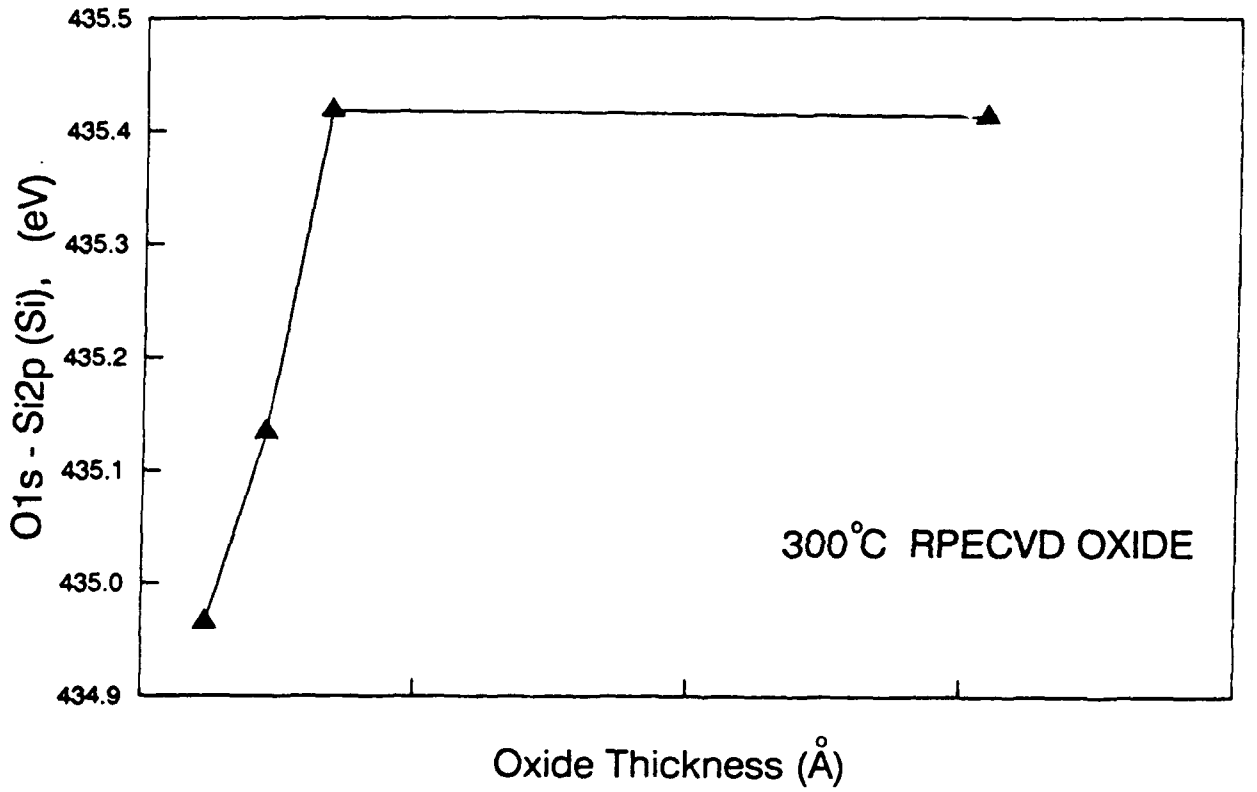

Figure 7 Binding energy differences as a function of oxide thickness from the interface: (a) between Si-2*p* (SiO_2) and the Si-2*p* (Si) signals, and (b) between O-1*s* and the Si-2*p* (Si) signals. The Si-2*p* (Si) position is taken to be that of the composite peak including both spin orbit components.

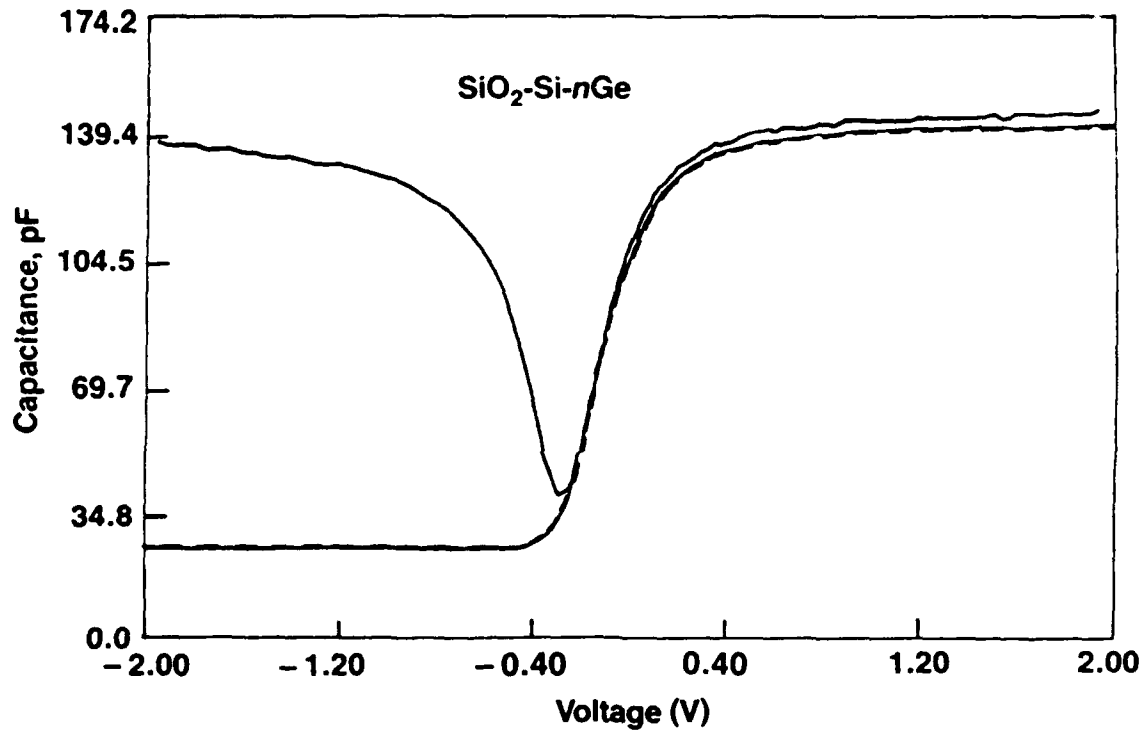

Figure 8 Quasi-static and high-frequency (1 MHz) capacitance-voltage characteristics from a MIS structure on *n*-Ge using the composite (150 Å)SiO_2 - (~20 Å)Si dielectric. The mid-gap interface state density is 5×10^{10} cm^{-2} eV^{-1}. The dotted high-frequency retrace shows no hysteresis.

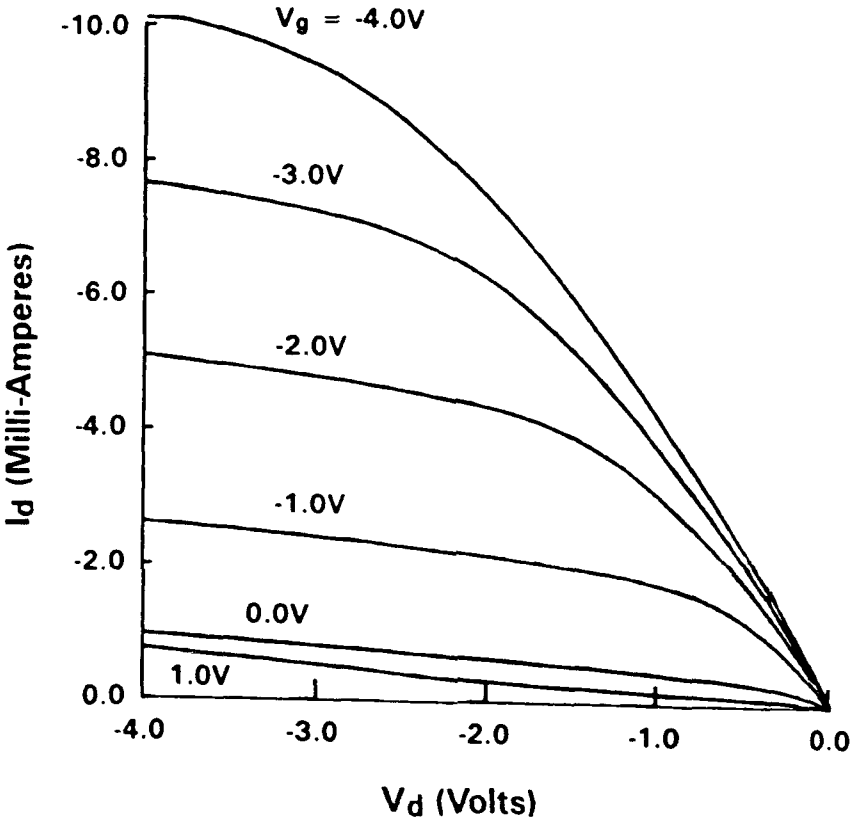

Figure 9 Transistor characteristics [drain-current (I_d) *versus* drain-voltage, (V_d) for different gate biases (V_g)] from an inversion-mode *p*-channel Ge MISFET fabricated using the composite SiO_2-Si dielectric. The gate length is 2 μm and the gate width is 50 μm. The measurements were obtained with a ramp rate of 1.0 V s^{-1}. The channel transconductance is 52 mS mm^{-1}. The peak effective channel hole mobility is 430 cm^2 V^{-1} s^{-1}.